lying in a second plane above the first plane,

each of the second level lines being disposed over a respective one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines;

a dielectric layer disposed between the first and second levels of conductive lines;

an array of vias arranged such that the first level line and the second level line of each of the at least four line pairs is connected by at least a respective plurality of vias, thereby forming an array of at least four parallel capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

12. The capacitor of claim 1, wherein each respective plurality of vias of the at least four line pairs of the at least four parallel capacitor plates is arranged opposite a next said respective plurality of vias, with identical spacing of vias in each plurality of vias.